(54) Titre : FILTRE ACCORDE DIRECTEMENT ET METHODE POUR ACCORDER UN FILTRE DIRECTEMENT
(54) Title: DIRECTLY TUNED FILTER AND METHOD OF DIRECTLY TUNING A FILTER
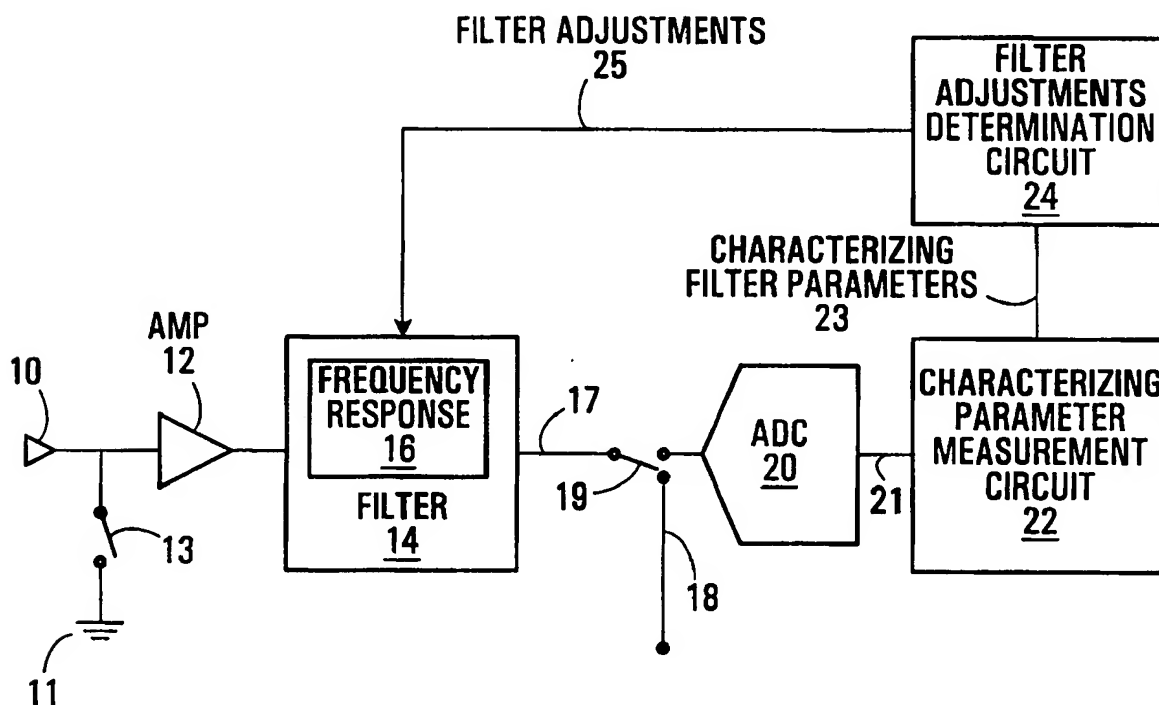
(57) Abrégé/Abstract:
A Method for filter tuning using direct digital sub-sampling is provided. The tuning is accomplished in the digital domain by determining the filter characteristics from the shape of the transfer function. The input signal (1) is passed through the filter (3) and is then sub-sampled by and Analog-to-digital Converter (ADC) (5). The sub-sampled signal (6) is then processed in the digital domain using a digital circuit (7) that is used to determine the center frequency (Fc) and Quality factor (Q) and/or other important filter parameters. The Fc, Q and/or other important filter parameters are then adjusted by generating digital control signals (8) that can be converted to analog signals (10) using Digital-to-analog Converters (DACs) (9).

50200-2

Abstract

A Method for filter tuning using direct digital sub-
sampling is provided. The tuning is accomplished in the
5 digital domain by determining the filter characteristics from
the shape of the transfer function. The input signal (1) is
passed through the filter (3) and is then sub-sampled by and
Analog-to-digital Converter (ADC) (5). The sub-sampled signal
(6) is then processed in the digital domain using a digital
10 circuit (7) that is used to determine the center frequency (Fc)
and Quality factor (Q) and/or other important filter
parameters. The Fc, Q and/or other important filter parameters
are then adjusted by generating digital control signals (8)
that can be converted to analog signals (10) using Digital-to-
15 analog Converters (DACs) (9).

Directly Tuned Filter and Method of Directly Tuning a Filter

Field of the Invention

The invention relates to the tuning of filters such as integrated circuit (IC) filters. In particular, it relates

5   to tuning of high frequency, high Q continuous time analog filters.

Background of the Invention

Recent research on radio frequency integrated circuits (RFICs) has focused on the development of fully

10   integrated radio receivers. There is an ongoing search for architectures that can deliver high selectivity and sensitivity, all at low cost and power consumption. It is well understood that the super-heterodyne architecture, with a high IF frequency, although difficult to integrate, has major

15   advantages in terms of image rejection and selectivity. A major design hurdle for integrating the super-heterodyne receiver is on chip filtering. The architecture typically requires one or more high Q filters to provide good selectivity. This has been traditionally accomplished with

20   relatively expensive off chip ceramic or Surface Acoustic Wave (SAW) filters. Extensive research has been done in the area of active on chip filtering. Much of the work is in the area of Gm-C filtering. It has been shown that at high frequencies, the use of on-chip Q-enhanced LC filters can have an advantage

25   over the typical Gm-C filter in terms of power and dynamic range. Q-enhanced filters are easily integrated into standard technologies and are capable of operation at very high frequencies. The Q-enhanced LC filter is also easily tunable in both frequency and Q and its circuit topology is inherently

30   simple. Research with Q-enhanced LC filters has explored

50200-2

- 2 -

several simple prototypes and higher order filters have also
been investigated.

Precise tuning of high Q integrated circuit filters
is essential for their correct operation. This is difficult or
5   impossible to achieve using manual tuning methods because
manual tuning methods cannot adequately accommodate
environmental variations such as temperature or power supply
changes. Master-Slave tuning suffers from component mismatch
and disparate circuit noise in the master and slave circuits.

10   Another existing method of tuning continuous time
filters has been proposed in U.S. Pat. No. 5,949,832 which
issued September 7, 1999, in which a communications signal is
decoded, and a change in the bit error rate of the decoded
signal compared to previous bit error rate is used to adjust
15   the filter bandwidth. U.S. Pat. No. 5,945,889 which issued
August 31, 1999, and U.S. Pat. No. 6,266,522 which issued July
24, 2001 provide solutions which are principally aimed at lower
frequency filters using Nyquist sampling.

Summary of the Invention

20   Methods of directly tuning an analog filter are
provided. Advantageously, the characteristics of a filter to
be adjusted can be determined by amplifying and shaping the
input spectrum of the filter thereby eliminating the need for
an input reference frequency signal.

25   The present invention preferably relies on sub-
sampling of the filter output which allows the system to tune
higher frequency signals using lower power sub-sampling ADCs.
In some embodiments, applying the filter function directly to
the input signal allows the input signal to be received

50200-2

- 3 -

continuously even while the filter is being tuned. This
increases the data transfer rate of the filter and adds
flexibility to the overall system implementation.

5   One broad aspect of the invention provides a method
of tuning an analog filter. The method involves: a) filtering
an input signal with the analog filter to produce a filtered
signal, the input signal being such that the filtered signal
has a frequency response representative of that of the analog
filter; b) performing analog-to-digital conversion on the
10   filtered signal to produce filtered signal digital samples; c)
processing the filtered signal digital samples to determine at
least one characterizing filter parameter; and adjusting the
filter based on at least one characterizing filter parameter.

In some embodiments, the method further involves
15   providing the input signal with a substantially flat spectral
density.

In some embodiments, the method further involves
disconnecting a normal input to the filter, and connecting the
filter to the input signal with the substantially flat spectral
20   density.

In some embodiments, the method further involves
performing amplification prior to performing analog-to-digital
conversion. This may be done before or after filtering.

In some embodiments, the characterizing filter
25   parameters comprise at least center frequency and Q.

In some embodiments, the method further involves: e)
repeatedly performing steps (a) through (d) until the
characterizing filter parameters satisfies at least one
objective.

50200-2

- 4 -

In some embodiments, the at least one objective comprises a respective predetermined range within which each characterizing filter parameter must fall.

In some embodiments, the method further involves: e) 5 repeatedly performing steps (a) through (d) until the center frequency and Q satisfy at least one objective.

In some embodiments, the at least one objective comprises a respective predetermined range within which each characterizing filter parameter must fall.

10 In some embodiments, the method is adapted to tune the filter periodically. In this case, the method involves i) performing steps a) through e); ii) disabling the method; wherein steps i) and ii) are performed at a predetermined update rate.

15 In some embodiments, the method is adapted to tune the filter periodically. In this case, the method involves: i) performing steps a) through e); ii) disabling the method; wherein steps i) and ii) are performed continuously.

In some embodiments, the filter is an on-chip Q 20 enhanced LC filter.

Another broad aspect of the invention provides a method of tuning a multi-stage analog filter. The method involves: a) setting characterizing parameters of all of filter stages of the multi-stage analog filter except one filter stage 25 to default values; b) filtering an input signal with the multi-stage analog filter to produce a filtered signal, the input signal being such that the filtered signal has a frequency response representative of that of the multi-stage analog filter; c) performing analog-to-digital conversion on the

filtered signal to produce filtered signal digital samples; d) processing the filtered signal digital samples to determine at least one characterizing filter parameter of the one filter stage; e) adjusting the one filter stage based on the at least

5 one characterizing filter parameters; repeating steps b) through e) to adjust the characterizing filter parameters of each other filter stage.

Another broad aspect of the invention provides an apparatus having an analog filter adapted to filter an input

10 signal to produce a filtered signal, the input signal being such that the filtered signal has a frequency response representative of that of the analog filter; an analog-to-digital converter adapted to sample the filtered signal to produce filtered signal digital samples; a digital circuit

15 adapted to process the filtered signal digital samples to determine at least one characterizing filter parameter and to adjust the filter based on the at least one characterizing filter parameter.

In some embodiments, the apparatus has a switch for

20 disconnecting a normal input to the filter, and connecting the filter to an input signal with a substantially flat spectral density.

In some embodiments, the apparatus has an amplifier adapted to perform amplification prior to performing analog-to-

25 digital conversion.

Brief Description of the Drawings

Preferred embodiments of the invention will now be described with reference to the attached drawings in which:

Figure 1 is a block diagram of a filter and tuning system provided by an embodiment of the invention;

Figure 2 is an example Q enhanced filter schematic with frequency and Q control signals;

5 Figure 3 is a block diagram of another filter and tuning system provided by an embodiment of the invention;

Figure 4 is a flow diagram of a method of tuning a filter provided by an embodiment of the invention; and

Figure 5 is a plot of results of Q tuning over time
10 for an example implementation.

Detailed Description of the Preferred Embodiments

The present invention now will be described more fully with reference to the accompanying drawings, in which embodiments of the invention are shown. The invention may be
15 embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, like
20 numbers refer to like elements throughout.

Referring now to Figure 1, a first example of a digitally tuned filter arrangement is shown. An input signal 10 is shown input to an amplifier 12 which is connected to an analog filter 14. The input to the amplifier (AMP) 12 can
25 alternatively be connected to ground 11 under control of switch 13. The filter 14 has an output 17 which is connectable either to an analog-to-digital converter (ADC) 20 or to an output 18 of the arrangement under the control of a switch 19.

Alternatively, if the output of the filter 14 is to be sampled in any case, then there is no need for switch 19. The output 21 of the ADC 20 is input to a digital domain characterizing parameter measurement circuit 22 which outputs characterizing

5   filter parameters 23 to a filter adjustment determination circuit 24. The filter adjustment determination circuit 24 outputs filter adjustments 25.

The filter 14 is any analog filter requiring adjustment. The frequency response of the filter is indicated

10   at 16. In a preferred embodiment, the filter is a bandpass filter but other transfer characteristics may be employed. It is to be understood that, in general, filters that have transfer characteristics that are adjustable may be used with the present invention. The invention is particularly suited to

15   high frequency applications. 500 MHz and 2.4 GHz are two example center frequencies. The filter might for example be an on-chip Q enhanced LC bandpass filter.

Circuits 22,24 may be implemented in any suitable form, using for example separate general purpose or specific

20   processors, a combined or specific general purpose processor, a DSP, ASIC, FPGA to name a few examples.

In operation, when the input to the amplifier 12 is connected to ground 11 under control of switch 13, the input to the amplifier 12 becomes a low amplitude white noise signal.

25   This is amplified by amplifier 12 to produce an amplified signal having a substantially flat power spectral density. The amplified signal is filtered by the filter 14 to produce at the filter output 17 a signal having a power spectral density which is proportionally representative of the frequency response 16

30   of the filter 14.

- 8 -

The ADC 20 performs analog-to-digital conversion and produces an output 21 consisting of a sequence of digital samples. In a preferred embodiment, rather than performing ADC over a frequency range spanning from base band to the maximum
5 frequency of the filter, sub-sampling is performed using an ADC operable over a range at least as large as the bandwidth of the filter 14.

The sampled signal 21 is then processed in the digital domain using the characterizing parameter measurement
10 circuit 22. The characterizing parameter measurement circuit 22 processes the sampled signal 21 to determine the set of characterizing filter parameters 23 in respect of the filter 14.

Once the characterizing filter parameters 23 are
15 determined, the filter adjustment determination circuit 24 decides on how best to adjust the filter such that the characterizing filter parameters satisfy objectives for the filter. In one embodiment, the filter 14 is equipped to have analog filter adjustment inputs 25 that directly adjust a
20 respective filter element for each characterizing parameter. This may for example involve determining digital control signals that are converted to analog signals using digital-to-analog converters.

It is to be understood that the filter parameters are
25 not totally independent and it may be necessary to have a relatively complex algorithm to adjust their values. The use of a digital tuning algorithm is therefore highly desirable. It is also to be understood that the tuning method is a form of direct tuning as the filter itself is tuned without the use of
30 a master filter or voltage controlled oscillator (VCO). The tuning of the filter requires the digitization of the filter

output. The filter amplifies and shapes the input signal to
the filter transfer function. In the above described example,
to facilitate direct tuning, the input signal and its
potentially large unwanted spectral components are removed
5 during tuning by using the input switch 13. More generally,
some method of attenuating/removing the input signal is
required. In another implementation, this can be accomplished
by lowering the gain of the amplifier. The resulting frequency
shaping by the filter may be amplified during tuning to give
10 sufficient Signal-to-Noise Ratio (SNR) in the ADC 20 so that
the shape can be resolved in the characterizing parameter
measurement circuit 22.

It is noted that tuning of the filter at a
sufficiently high update rate can help mitigate low frequency
15 1/f noise by resetting characterizing filter parameters
consisting of Fc and Q at a regular interval. The required
update depends on a given environment, and depends for example
on how fast the parameters of the filter are drifting, and how
accurate the filter is required to be. Other example
20 characterizing parameters include pass-band ripple, stop-band
roll-off, bandwidth, and basically any parameter that can be
compared against filter objectives.

The illustrated embodiment shows an amplifier,
typically a low noise amplifier (LNA) before the filter, but
25 this is not necessarily a requirement. Such an LNA is
typically included in receivers for proper reception of the
signal, and is necessary to improve the sensitivity of the
system in which case it does not have much to do with the
actual tuning. Alternatively, or additionally, an amplifier
30 may be provided after the filter. In respect of the tuning of
the filter, the reason for the amplifier after the filter is to

amplify the shaped noise from the filter so that it can be
seen by the ADC (i.e. is within the ADC's Dynamic Range). In
order to accomplish this, the signal will likely need to be
amplified unless an ADC with a large SNR is employed (eg. 60dB

5   or more). The noise can be amplified before going into the
filter as illustrated in Figure 1 and get the same effect, but
the filter would then have to deal with a much larger signal,
which is difficult for some integrated types of filters. In
many cases it is better to just ground the input to the filter

10 and have an RF or IF amplifier after the filter but before the
ADC.

    Q enhanced LC filters typically have a transfer
characteristic that is adjustable by varying the
transconductance of the negative gm transconductor and the

15 capacitance of the LC tank. This may be accomplished in a
number of ways as Q enhanced LC filters may have a wide variety
of configurations. A typical Q enhanced filter is illustrated
in Figure 2. In this example, the center frequency of the
filter passband is dependent on the value of the inductors 32

20 and capacitors in the tank circuit. A well-known technique for
adjusting the capacitance is to use a variable capacitance
varactor 33 as the tank capacitance. Typically, the Q of the
filter can be adjusted by varying the transconductance of the
negative gm transconductor 31. Both of these parameters can be

25 adjusted by varying an externally-applied control signal to
control biasing point VFc 34 and VQ 35, as for example
described in: Pipilos, S., Tsividis, Y.P., Fenk, J., Papananos,
Y., "A Si 1.8 GHz RLC Filter with Tunable Center Frequency and
Quality Factor," IEEE Journal of Solid State Circuits, vol. 31,

30 n. 10, Oct. 1996.

A more detailed implementation suitable for the filter of Figure 2 for example is shown in Figure 3 where elements which are common with Figure 1 have been identically numbered. In this case, the filter 14 has a bandpass frequency
5 response, characterized by characterizing filter parameters Q and center frequency Fc. The characterizing parameter measurement circuit 22 and the filter adjustment determination circuit 24 of Figure 1 are shown implemented as a single digital circuit 27. For example, Fc may be determined by
10 performing an FFT of the sampled data, removing the narrow band desired signal and any other interfering signals, smoothing the amplified noise if necessary and finding the peak of the resultant frequency response. A more efficient approach is to replace the FFT with programmable digital filters at know
15 frequencies. The Q can be determined by measuring the 3dB bandwidth of the resultant frequency response. This is one example of a method for resolving the filter parameters. Depending on speed, accuracy and power requirements other methods may be employed.

20   In this case, the digital circuit 27 produces digital control signals for the Q and Fc of the filter 24. Adjustments to the Q and Fc inputs are determined, and these are converted to analog control signals 25 using a pair of digital-to-analog converters (DACs) 40.

25   Figure 4 is an example flow diagram of the tuning process in operation. When it is time to update the filter parameters, either when the filter is initially powered up, or when an update period has expired, the input is connected to the white noise source (ground) and is shaped to the filter
30 transfer function in step 4-1. Next the filter output is sub-sampled at step 4-2, and the filter parameters, such as Fc and

- 12 -

Q, are calculated at step 4-3. Filter parameter adjustment
then takes place. In this example, this involves performing a
test at step 4-4 to see if the filter parameters are within
predetermined ranges. If the filter parameters are all within
5 range (yes path step 4-4) then the tuning cycle is complete and
there is a predetermined update delay, which is zero for
continuous tuning, before the tuning cycle is performed again
beginning at step 4-1. If the filter parameters are not within
range (no path, step 4-4) then the filter control signals are
10 adjusted at step 4-5 and the initial tuning process is begun
again at step 4-1. Preferably, continuous tuning is employed
until the filter parameters are all within range.

In the above described embodiment, re-tuning is
triggered by a delay time or by system power up, but more
15 generally this could also be triggered by some other event in
the system. In one embodiment, the system is configured to re-
tune upon detection of a reduction in the quality of the
filtered signal. This quality detection may be performed in
the digital circuitry.

20 The illustrated embodiments have assumed that the
input is connected to ground so that a white noise signal is
input to the amplifier and filter, and such that the filtered
output has a power spectrum which is representative of that of
the filter. In another embodiment, if there is sufficient
25 knowledge of the frequency characteristics of the actual input
signal (signal 10 of Figure 1), then the frequency response of
the filter can be determined using this knowledge without
requiring the white noise input. This approach will allow
continuous tuning during the operation of the filter.

30 The illustrated embodiments have involved tuning of a
single filter. In another embodiment, the approach is adapted

50200-2

- 13 -

for use in a cascaded filter arrangement of two or more filter stages. In this approach, all of the filter stages are initially set to low Q (or to some other default state), then one of the filter stages is tuned using the described method.
5 Then, tuning is performed on the subsequent filter stages in sequence.

In another embodiment, the input signal may pass through a mixer before the ADC. When the filter is implemented as part of a receiver, this would typically be the case, with a
10 mixer being employed to bring a received RF signal into an IF band that is then filtered and analog-to-digital converted.

As indicated previously, sub-sampling in the ADC can be employed so that a reduced input bandwidth ADC is required. For this IF example, it is possible to use sub-sampling to
15 sample the signal at a lower frequency than the carrier, provided that the sampling frequency obeys the Nyquist theorem with respect to the bandwidth of the signal. This allows the use of a low frequency sampling clock and ADC. An important consideration is that the input bandwidth of the ADC has to
20 accommodate the high frequency IF signal. The correct conversion of the desired band depends on the following criteria:

$$kf_s < f_h, f_l < (k+1/2)f_s \text{ where } 2 < k < \frac{f_h}{f_h - f_l}$$

In the above equations, f_s is the sampling frequency, f_h and f_l
25 are the highest and lowest frequencies within the desired band respectively and k is an integer. The use of IF sampling allows the signal to be mixed down and processed in the digital domain, providing potentially significant power savings as well as increased flexibility in the receiver.

Noise folding or aliasing has the effect of folding 2×m noise images, where m is the over-sampling ratio, into the band of interest. By using a high Q bandpass filter at the input of the ADC this problem can be eliminated.

5   For example, a Q of 500 and center frequency of 500 MHz may be used. A sampling frequency of 80 MHz is chosen giving a sub-sampling ratio of 6. The largest noise images occur at +/- 40 MHz and are attenuated by 37 dB. Since these images are much larger than all other noise images, we can

10   approximate the amount of folding by:

$$\frac{N_{folding}}{N_{in-band}} \approx 10\log(2) - 37dB = -34dB$$

which means the added noise is insignificant. Wide-band noise from the ADC sample and hold circuit is not filtered by the IF filter and so this noise will see the entire effect of the sub-

15   sampling. In general, for a low precision ADC (i.e. limited dynamic range requirement) this noise will be much lower than the quantization noise of the converter. The sub-sampling converter will also produce images of blocking signals at each multiple of the sampling frequency.

20   Simulation Results

The ADC used in a test setup was a Texas Instruments TLV5580, which is an 8 bit 80 MSPS converter with an analog input bandwidth of 700 MHz. The digital tuning was accomplished using an FPGA and a PC running Matlab. A sampling

25   frequency of 80 MSPS gives a usable tuning range of 40 MHz. This means that the filter has to be calibrated to ensure the initial frequency is within that 40 MHz range. A 1024 point 8 bit FFT was implemented in an Altera Apex20K400 FPGA using 20K gates, 4Kbits of sin/cos ROM and 16Kbits of RAM. The FFT is

50200-2

- 15 -

performed in 52uS using an 80MHz clock and gives a resolution of 78 kHz.

Figure 5 shows an example of the variations with time of a filter tuned to a Q of 500 for closed loop tuning 50
5 according to an embodiment of the invention, and for open loop tuning 52. The closed loop tuning includes a filter refresh tuning of the Q every 300 milliseconds. In the example the RMS value of 2^{13} samples are used to calculate the Q, which takes a total of 102 μs. The resulting Q accuracy is +/- 0.68 % (2σ).

10   While the present invention has been illustrated and described with reference to specific embodiments, further modifications and improvements will occur to those skilled in the art. It is to be understood, therefore, that this invention is not limited to the particular forms illustrated,
15 for example, other types of filters or tuning algorithms could be used. It is intended that these claims cover all modifications that do not depart from the spirit and scope of this invention.

We claim:

1.   A method of tuning an analog filter comprising:

a) filtering an input signal with the analog filter to produce a filtered signal, the input signal being such that
5   the filtered signal has a frequency response representative of that of the analog filter;

b) performing analog-to-digital conversion on the filtered signal to produce filtered signal digital samples;

c) processing the filtered signal digital samples to
10 determine at least one characterizing filter parameter;

d) adjusting the filter based on the at least one characterizing filter parameter.

2.   A method according to claim 1 further comprising:

providing the input signal with a substantially flat
15 spectral density.

3.   A method according to claim 2 further comprising:

disconnecting a normal input to the filter, and connecting the filter to the input signal with the substantially flat spectral density.

20 4.   A method according to claim 3 further comprising performing amplification prior to performing analog-to-digital conversion.

5.   A method according to claim 1 wherein the characterizing filter parameters comprise at least center
25 frequency and Q.

6.   A method according to claim 1 further comprising:

50200-2

- 17 -

e) repeatedly performing steps (a) through (d) until the characterizing filter parameters satisfies at least one objective.

7.   A method according to claim 6 wherein the at least
5   one objective comprises a respective predetermined range within which each characterizing filter parameter must fall.

8.   A method according to claim 5 further comprising:

e) repeatedly performing steps (a) through (d) until the center frequency and Q satisfy at least one objective.

10 9.   A method according to claim 8 wherein the at least one objective comprises a respective predetermined range within which each characterizing filter parameter must fall.

10.   A method according to claim 6 adapted to tune the filter periodically, the method comprising:

15   i) performing steps a) through e);

ii) disabling the method;

wherein steps i) and ii) are performed at a predetermined update rate.

11.   A method according to claim 6 adapted to tune the
20 filter periodically, the method comprising:

i) performing steps a) through e);

ii) disabling the method;

wherein steps i) and ii) are performed continuously.

12.   A method according to claim 1 wherein the filter is
25 an on0chip Q enhanced LC bandpass filter.

- 18 -

13.   A method of tuning a multi-stage analog filter comprising:

a) setting characterizing parameters of all of filter stages of the multi-stage analog filter except one filter stage
5 to default values;

b) filtering an input signal with the multi-stage analog filter to produce a filtered signal, the input signal being such that the filtered signal has a frequency response representative of that of the multi-stage analog filter;

10   c) performing analog-to-digital conversion on the filtered signal to produce filtered signal digital samples;

d) processing the filtered signal digital samples to determine at least one characterizing filter parameter of the one filter stage;

15   e) adjusting the one filter stage based on the at least one characterizing filter parameters;

repeating steps b) through e) to adjust the characterizing filter parameters of each other filter stage.

14.   An apparatus comprising:

20   an analog filter adapted to filter an input signal to produce a filtered signal, the input signal being such that the filtered signal has a frequency response representative of that of the analog filter;

an analog-to-digital converter adapted to sample the
25 filtered signal to produce filtered signal digital samples;

a digital circuit adapted to process the filtered signal digital samples to determine at least one characterizing

filter parameter and to adjust the filter based on the at least one characterizing filter parameter.

15.   An apparatus according to claim 14 wherein the input signal has a substantially flat spectral density.

5 16.   An apparatus according to claim 14 further comprising:

        a switch for disconnecting a normal input to the filter, and connecting the filter to an input signal with a substantially flat spectral density.

10 17.   An apparatus according to claim 14 further comprising:

        an amplifier adapted to amplify the filtered signal prior to performing analog-to-digital conversion.

18.   An apparatus according to claim 14 wherein the
15 characterizing filter parameters comprise at least center frequency and Q.

19.   An apparatus according to claim 14 adapted to repeatedly adjust the filter until each characterizing filter parameter satisfies at least one objective.

20 20.   An apparatus according to claim 14 adapted to adjust the filter until each characterizing filter parameter falls within a respective predetermined range, after which no updating is performed until an update period has passed.

21.   An apparatus according to claim 14 wherein the filter
25 is a high Q bandpass filter.

22.   An apparatus according to claim 14 wherein the filter is an on-chip Q enhanced LC bandpass filter.
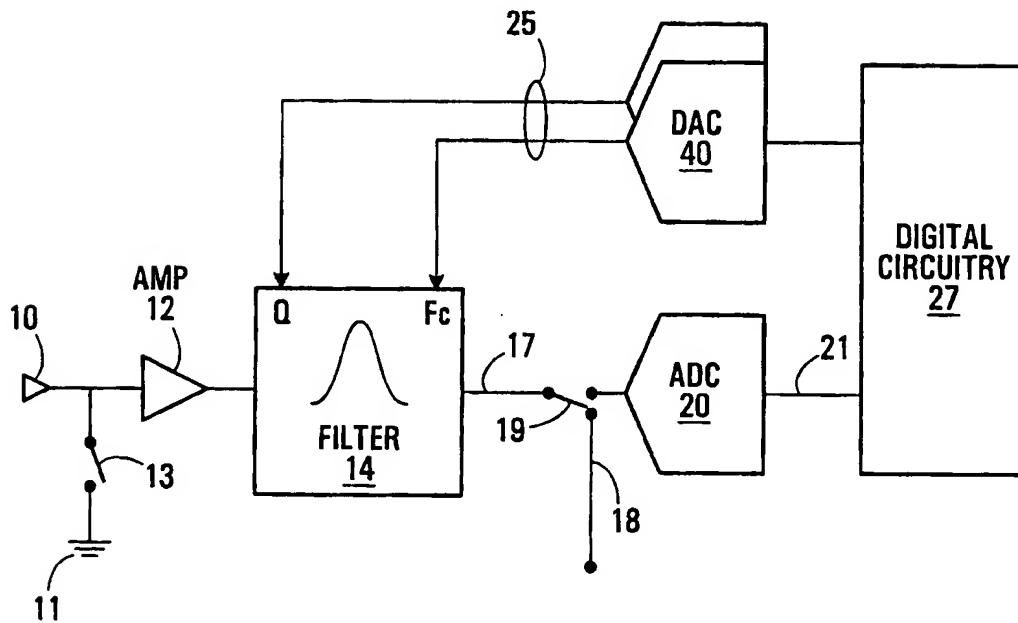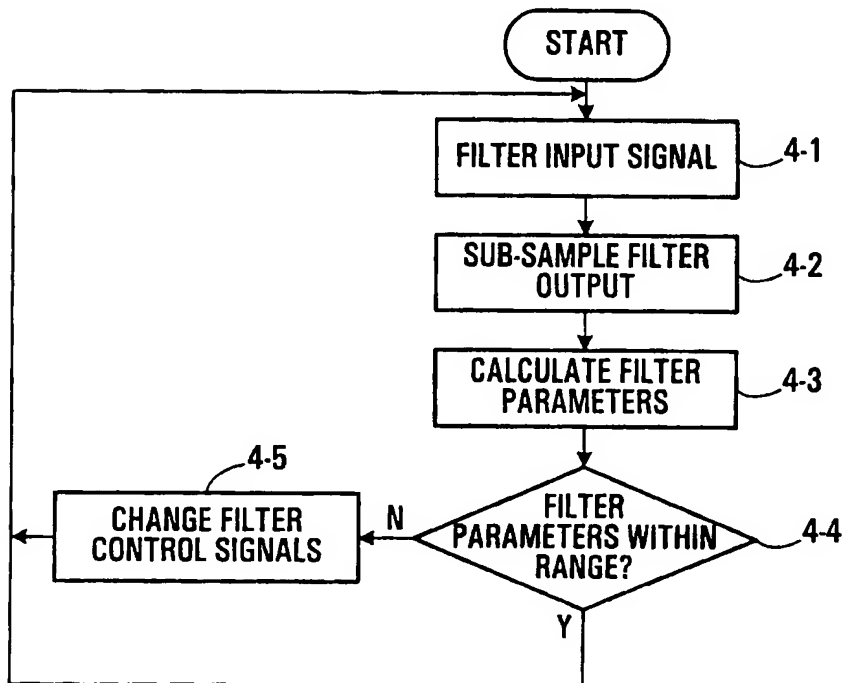
50200-2

- 20 -

23.   An apparatus according to claim 14 wherein the ADC is adapted to sub-sample the filter output with a bandwidth at least as great as a bandwidth of interest of the filter.
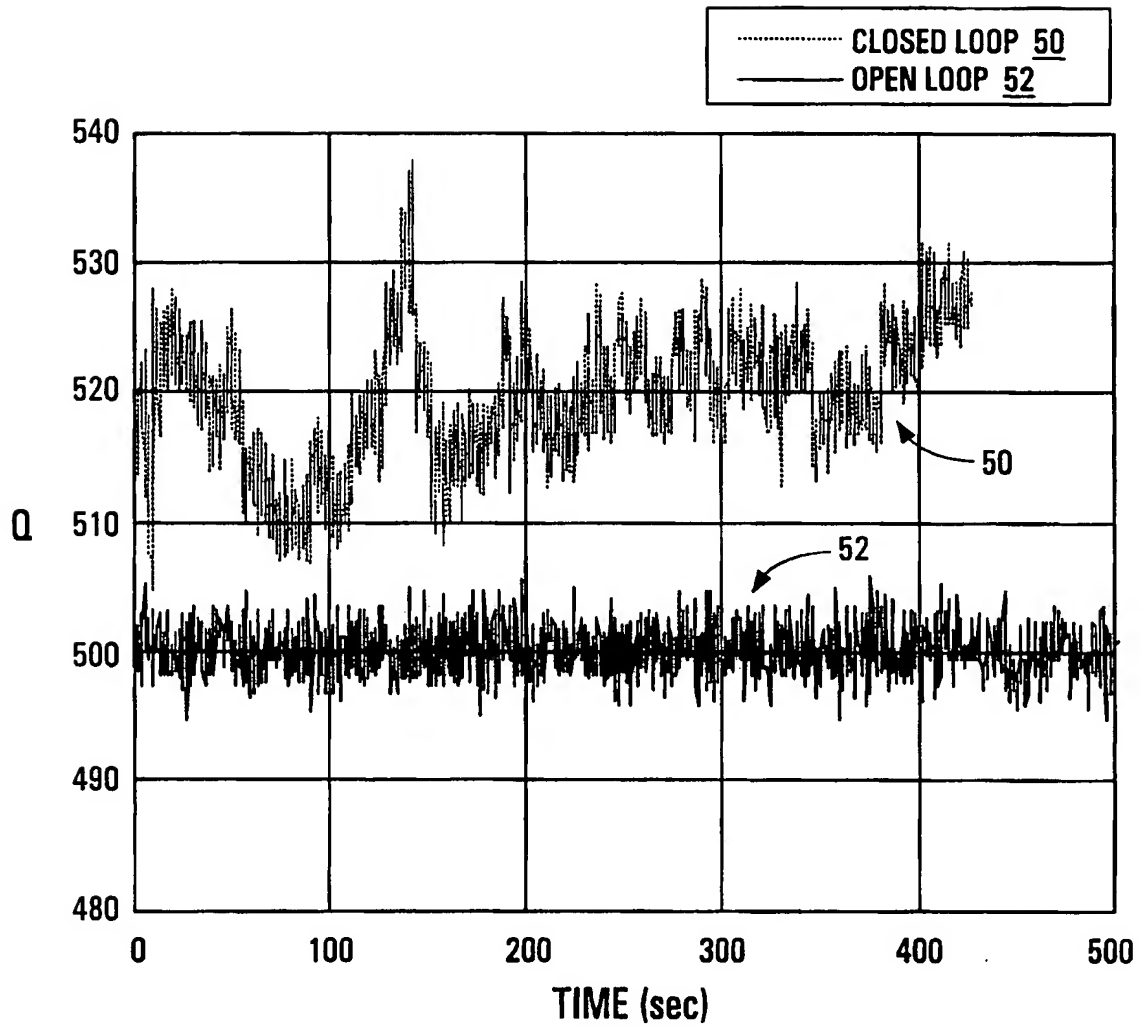
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1/3

FIG. 1

FIG. 2

2/3

FIG. 3

FIG. 4

FIG. 5

FILTER ADJUSTMENTS
25

FILTER
ADJUSTMENTS
DETERMINATION
CIRCUIT
24

CHARACTERIZING
FILTER PARAMETERS
23

AMP
12

10

FREQUENCY
RESPONSE
16

FILTER
14

17

19

ADC
20

21

CHARACTERIZING
PARAMETER
MEASUREMENT
CIRCUIT
22

13

18

11